

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A bias circuit having a start-up circuit, comprising:
a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and
a start-up circuit part having a capacitor connected between the output node and a common node connecting gates of MOS transistors constructing the current mirror circuit, wherein the MOS transistors include a first PMOS transistor and a second PMOS transistor and the bias circuit part includes:
the first PMOS transistor having a source thereof connected to the power source voltage;
the second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the common node, and having a source thereof connected to the power source voltage;
a first NMOS transistor having a drain and a gate thereof connected to a drain of the first PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the second PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between the source of the second NMOS transistor and the grounded power source,

wherein the source of the second NMOS transistor is connected to a body of the second NMOS transistor; and

wherein the bias circuit comprises the start-up circuit part for improving stability characteristics of the constant bias voltage at a high frequency range and eliminating noise from the power source voltage.

2. (canceled).

3. (currently amended): A bias circuit having a start-up circuit, comprising:

a bias circuit part using a cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an applied power source voltage; and

a start-up circuit part for actuating the bias circuit part upon an initial application of the power source voltage, the start-up circuit part including:

a first capacitor connected between a first common node connecting in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit and a second common node connecting in common gates of second MOS transistors constructing a second single-stage current mirror circuit; and

a second capacitor connected between the second common node and the output node, wherein the first MOS transistors include a first PMOS transistor and a second PMOS transistor, the second MOS transistors include a third PMOS transistor and a fourth PMOS transistor and the bias circuit part includes:

the first PMOS transistor having a source thereof connected to the power source voltage;

the second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the first common node, and having a source thereof connected to the power source voltage;

the third PMOS transistor having a source thereof connected to a drain of the first PMOS transistor;

the fourth PMOS transistor having a gate and a drain thereof connected to a gate of the third PMOS transistor to form the second common node, and having a source thereof connected to the drain of the second PMOS transistor;

a first NMOS transistor having a drain and a gate thereof directly connected to a drain of the third PMOS transistor to form the output node, and having a source thereof connected to a grounded power source; and

a second NMOS transistor having a drain thereof directly connected to the drain of the fourth PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor,

wherein a resistor is connected between a source of the second NMOS transistor and the grounded power source, and

wherein the bias circuit comprises the start-up circuit part for improving stability characteristics of the constant bias voltage at a high frequency range and eliminating noise from the power source voltage.

4. (canceled).

5. (previously presented): The bias circuit as claimed in claim 1, wherein the output node outputs the constant bias voltage out of the bias circuit.

6. (previously presented): The bias circuit as claimed in claim 3, wherein the output node outputs the constant bias voltage out of the bias circuit.

7. (previously presented): The bias circuit as claimed in claim 1, wherein the output node outputs the constant bias voltage to another circuit outside the bias circuit.

8. (previously presented): The bias circuit as claimed in claim 3, wherein the output node outputs the constant bias voltage to another circuit outside the bias circuit.

9. (currently amended): A bias circuit having a start-up circuit, comprising:

a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output terminal node from a power source voltage as applied, and

a start-up circuit part having a capacitor connected between a base of the output terminal and a common node connecting gates of MOS transistors constructing the current mirror circuit,

wherein the MOS transistors include a first PMOS transistor and a second PMOS transistor and the bias circuit part includes:

the first PMOS transistor having a source thereof connected to the power source voltage;

the second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the common node, and having a source thereof connected to the power source voltage;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the first PMOS transistor to form the base of the output terminal, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the second PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between the source of the second NMOS transistor and the grounded power source,

wherein the source of the second NMOS transistor is connected to a body of the second NMOS transistor; and

wherein the bias circuit comprises the start-up circuit part for improving stability characteristics of the constant bias voltage at a high frequency range and eliminating noise from the power source voltage.

10. (canceled).

11. (currently amended): The bias circuit as claims in claim 1, wherein ~~the bias circuit comprises the start up circuit means for preventing prevent~~ transient states at a beginning of a supply of the power source voltage.

12. - 13. (canceled).

14. (new): A bias circuit having a start-up circuit, comprising:

a bias circuit part using a cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an applied power source voltage; and

a start-up circuit part for actuating the bias circuit part upon an initial application of the power source voltage, the start-up circuit part including:

a first capacitor connected between a first common node connecting in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit and a second common node connecting in common gates of second MOS transistors constructing a second single-stage current mirror circuit; and

a second capacitor connected between the second common node and the output node, wherein the first MOS transistors include a first PMOS transistor and a second PMOS transistor, the second MOS transistors include a first NMOS transistor and a second NMOS transistor and the bias circuit part includes:

the first PMOS transistor having a source thereof connected to the power source voltage;

the second PMOS transistor having a gate thereof connected to a gate and a drain of the first PMOS transistor and a drain of the first NMOS transistor to form the first common node, and having a source thereof connected to a resistor, wherein the resistor is connected between the source of the second PMOS transistor and the power source voltage;

the first NMOS transistor having a drain thereof connected to the drain and the gate of the first PMOS transistor and the gate of the second PMOS transistor;

the second NMOS transistor having a gate and a drain thereof connected to a drain of the second PMOS transistor and a gate of the first NMOS transistor to form the second common node, and having a source thereof connected to a drain and a gate of a fourth NMOS transistor;

a third NMOS transistor having a drain thereof directly connected to a source of the first NMOS transistor, and having a source thereof connected to a grounded power source; and

the fourth NMOS transistor having a drain and a gate thereof directly connected to the source of the second NMOS transistor and a gate of the third NMOS transistor to form the output node, and having a source thereof connected to the grounded power source, and

wherein a body of the first NMOS transistor and the second NMOS transistor are connected to the grounded power source.